REMARKS

Claims 1 to 31 are currently pending.

The Patent Office objected to the drawings under 37 C.F.R. 1.83(a). Figure 3 has been amended to show the features of claims 11, 22, 28, and 29. Claims 26 and 27 are illustrated in figure 1. Applicant believes that figures 2A to 2C sufficiently illustrate the limitations of claims 18 and 19. Claims 16, 30, and 31 are illustrated in replacement figure 3. Replacement drawing figure 3 shows an external memory, host bus adapters with processors, and at least one host bus adapter with a memory buffer as well as two controllers on a single card. The support for this amendment to Figure 3 is found on page 4, lines 4-5; page 6, lines 19-24; page 10, lines 10-14; page 13, lines 17-20; original claim 11; and/ or original figure 1. It is respectfully submitted no new matter has been added.

Certain claims have been amended to clarify the scope of Applicant's invention. Claims 1, 5, 6, 20, 23, 24, and 31 have been amended to clearly recite that whereas a first controller may be reset, any other controllers are not reset. This amendment is supported on page 7, lines 18-20, of Applicant's specification. The amendment to claim 23 is further supported by page 6, lines 15-17, of Applicant's specification. It is respectfully submitted that no new matter has been added.

The present invention solves prior art problems with multiple controllers in which "either all the controllers reset and there is a loss of access to storage devices during the simultaneous reset of the controllers, or only the defective controller resets and there is insufficient information to solve the defect" (page 2, lines 25-28, of Applicant's specification).

The Patent Office rejected claims 1-10, 13-15, 20, 21, 23, 24, and 29 under 35 U.S.C. 102(a) as being anticipated by the "Background of the Invention" (BOI).

For a claim to be anticipated by a reference, each and every element of the claim must be disclosed by that reference (MPEP 2131) unless the element is inherent.

Claim 1 recites "A computer program product stored on a computer readable storage medium for maintaining data access during failure of a first controller in a multiple controller storage subsystem, the storage subsystem having an array of data storage devices and at least one other controller for managing the data storage, comprising computer readable program code for performing saving internal state information by the first controller; pausing operation of the at

least one other controller; the at least one other controller saving internal state information without resetting at the time of pausing; and continuing operation of the at least one other controller."

Claim 20 recites "A method for maintaining data access during failure of a first controller in a multiple controller storage subsystem, the storage subsystem having an array of data storage devices and at least one other controller for managing the data storage, the method comprising the first controller saving internal state information; pausing operation of the at least one other controller; the at least one other controller saving internal state information at the time of pausing without resetting; and, continuing operation of the at least one other controller."

Claim 23 recites "An apparatus for maintaining data access during failure of a first controller in a multiple controller storage subsystem, the storage subsystem comprising at least one other controller for managing the data storage, the apparatus comprising the first controller comprising means for storing internal state information; and, the at least one other controller comprising means, responsive to failure of the first controller, for pausing operation, saving internal state information at the time of pausing without resetting, and continuing operation."

Claim 24 recites "A storage subsystem comprising at least two controllers for managing data storage, the at least two controllers coupled to at least one data storage device, the storage subsystem further comprising a first controller of the at least two controllers adapted for saving internal state information during a failure of the first controller; and, at least one other controller of the at least two controllers adapted for pausing operation, saving internal state information at the time of pausing, and continuing operation during the failure of the first controller, wherein only the first controller resets."

As noted in the BOI, a problem with the prior art, including that discussed in the BOI, is that the problem is "either all the controllers reset and there is a loss of access to storage devices during the simultaneous reset of the controllers, or only the defective controller resets and there is insufficient information to solve the defect." It is during such failures, the BOI teaches that access to the storage devices is prevented or insufficient information is saved so as to solve the defect or error. The BOI neither discloses nor suggests that a first controller's internal state information is saved and at least one other controller's internal state information is saved without resetting the at least one other controller. Thus, Claims 1, 20, 23, and 24 are allowable over the

prior art of record.

Because claims 1, 20, 23, and 24 are allowable, dependent claims 2-19, 21, 22, and 25-30 are also allowable.

The Patent Office rejected claims 11 and 28 under 35 U.S.C. 103(a) as being unpatentable over BOI. Claims 11 and 28 are allowable because they depend from allowable base claims 1 and 24, respectively.

The Patent Office rejected claims 16, 17, 22, 25, and 30 under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Otterness et al., U.S. Patent No. 6,601,138. Claims 16, 22, 25, and 30 are allowable because they depend from allowable base claims 1 or 24.

Claim 17 recites "A computer program product as claimed in claim 16, wherein during the at least one other controller pausing operation, saving internal state information at the time of pausing, and continuing operation, interrupts are disabled."

BOI discloses "The feature where a failing controller sends a stop message to other controllers is often disabled in the field because the systems are high availability systems" (page 2, lines 16-18, of Applicant's specification). The feature recited in BOI appears to concern an initial default setting in the system regarding whether to allow the propagation of stop messages and not the disabling of interrupts. Contrary to the assertion by the Patent Office on page 8, last four lines, of the Office Action mailed July 14, 2005, BOI does not appear to disclose or even suggest "interrupts are disabled" as recited in claim 17. Thus, claim 17 is allowable over the prior art of record for this additional reason.

The Patent Office rejected claim 18 under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Otterness, further in view of Skazinski et al., U.S. Patent No. 6,574,790.

Claim 18 recites "A computer program product as claimed in claim 16, wherein a flag is set in a host bus adapter during the saving of internal state information to prevent overlapping saves of internal state information in that adapter."

The Patent Office asserted, in paragraph 7, of the Office Action mailed July 14, 2005, (pages 9-10) "As per claim 18, the combination of BOI and Otterness teaches the claimed invention as described above. However, none of them clearly teach about setting a flag to prevent overlapping saves of internal state information in that adapter. Skazinski teaches that using alternate flag (see line 8, Table 6) which is set to equal to true ("1"), to indicate that an

alternate mirror entry 6000 is being used to perform the present mirror cache operation to prevent the problems with respect to mirror operation overlap (e.g., see Col. 22, lines 40-47). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Skazinski's step of setting the flag in the system taught by BOI and Otterness to avoid overlapping saves of internal state information in that adapter."

Skazinski does not disclose setting a flag to prevent overlapping saves of internal state data in that adapter. Skazinski also appears to be concerned with host write data (e.g., column 14, lines 35-48) and not state information, as claimed. Neither Otterness nor the BOI seem to disclose the use of flags. Thus, claim 18 is allowable over the prior art of record for this additional reason.

The Patent Office rejected claim 19 under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Otterness, further in view of Mason, Jr., et al., U.S. Published Patent Application No. 2003/0135674.

Mason discloses, in paragraph 0064, "FIG. 6 is a diagram illustrating how a Peripheral Component Interconnect (PCI) embodiment is connected between the device I/O interface circuitry on a host bus adapter 8 and a disk storage unit 3 utilizing a host I/O interface 7 cable at the front end of the storage management platform and a device I/O interface 2 cable at the back end. Note that the data flow to and from the host bus adapter 8 is over the I/O bus through the I/O cable 7. No data is transferred over the PCI bus 21. This embodiment, taken together with the PCI embodiment illustrated in FIG. 3 illustrate how each and every embodiment of the subject invention plugs into the I/O bus and not the system bus, regardless of whether the host end of the I/O bus is implemented as an I/O interface chip on a motherboard or an I/O interface ship on a host bus adapter that plugs into the system bus." Mason does not disclose or suggest that the host bus adapter saves information relating to an interface chip. Thus, claim 19 is allowable over the prior art of record for this additional reason.

The Patent Office rejected claims 12, 26, and 27 under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Oldfield et al., U.S. Published Patent Applications No. 2002/0133743.

Claim 26 is allowable because it depends from allowable claim 24.

Claim 12 recites "A computer program product as claimed in claim 1, wherein in addition

to the internal state information, at least one of the first controller and the at least one other controller save external memory data." Claim 27 recites "A storage subsystem as in claim 24, wherein the first controller and the at least one other controller share an external memory." BOI does not disclose or suggest an external memory and does not suggest or disclose a need for an external memory. The attempt to modify the BOI by Oldfield is impermissible hindsight reconstruction. Thus, claims 12 and 27 are allowable over the prior art of record for this additional reason.

The Patent Office rejected claim 31 under 35 U.S.C. 102(a) as being anticipated by DeKoning et al., U.S. Patent No. 5,933,824 hereinafter, DeKoning in view of BOI.

Claim 31 recites "A Fibre Channel Arbitrated Loop storage system comprising a first set of disk drives connected to a first set of loops, and a second set of disk drives redundant with the first set of disk drives and connected to a second set of loops; wherein a first adapter is connected to the first set of loops and a second adapter is connected to the second set of loops; each adapter being adapted for issuing a command to the other adapter to save internal status data without resetting and each adapter adapted for saving internal status data and resetting."

For a claim to be anticipated by a reference, each and every element of the claim must be disclosed by that reference (MPEP 2131) unless the element is inherent.

Because it is not clear if the Patent Office meant to reject claim 31 under 35 U.S.C. 102(a) or 35 U.S.C. 103(a) and the Patent Office acknowledged a difference not taught by DeKoning in claim 31, Applicant henceforth will treat the rejection of claim 31 as a 103(a) rejection over DeKoning in view of BOI.

Neither DeKoning nor the BOI disclose or suggest "each adapter being adapted for issuing a command to the other adapter to save internal status data without resetting and each adapter adapted for saving internal status data and resetting." In fact, BOI teaches away from this limitation since BOI (the prior art) has been identified as having a problem in that state data is lost on a controller's failover or insufficient state data is saved in a system when a controller fails to resolve a defect. DeKoning does not acknowledge a problem with error recovery or data storage access during a controller failover and so is not properly modifiable by the BOI. Thus, claim 31 is allowable over the prior art of record.

The Patent Office is respectfully requested to reconsider and remove the rejections of the

claims under 35 U.S.C. 102(a) or 103(a) based on BOI, Otterness, DeKoning, Oldfield, Skazinski, and Mason, alone or in combination, and to allow all of the pending claims 1-31 as now presented for examination. An early notification of the allowability of claims 1-31 is earnestly solicited.

Respectfully submitted:

Walter J. Malinowski August 31, 2005

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450.

8/31/2005 Elaine F. Mason

AMENDMENTS TO THE DRAWINGS:

The attached sheet of drawings includes changes to Fig. 3, and replaces the original sheet of Fig. 3 of drawings. In this Figure, an external memory is shown, each host bus adapter has a processor, and one host bus adapter has a memory buffer. Also, the two host bus adapters are shown on a single card. The support for these features is found on page 4, lines 4-5; page 10, lines 10-14; page 13, lines 17-20; and/ or figures 1 and 3.

Attachment: Replacement Sheets – 1 (Figure 3)
Annotated Sheets Showing Changes – 1 (Figure 3)

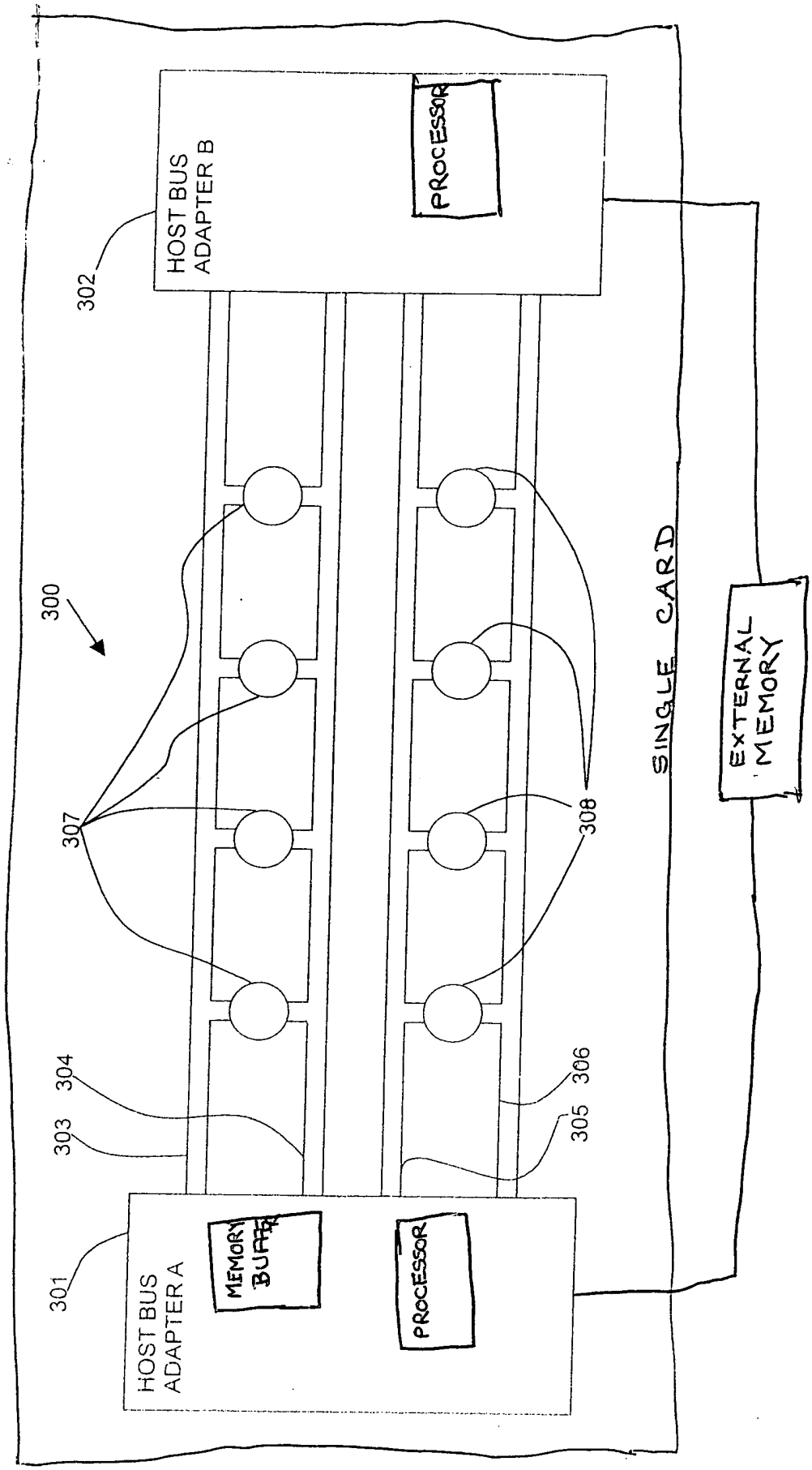

FIG. 3